

What is claimed is:

1. A computer chipset, comprising:

a first circuit to receive data from a computer processor
5 and process address information associated with data addresses in
the computer processor to determine a received data ordering of
the data based on the data addresses; and

a second circuit to reorder the data from said first circuit
into ordered packets each in a predetermined ordering and to
10 maintain the address information.

2. A computer chipset as in claim 1, wherein said first
circuit includes a token generator to receive and process the
address information of the data to generate tokens corresponding
15 to consecutive data packets, each token indicating at least the
received data ordering and addresses of data in a respective
packet.

3. A computer chipset as in claim 2, further comprising a
20 queue stage having a token queue and a data queue to respectively
receive and store the tokens and the data from said first
circuit, wherein said first and second circuits form a pipeline
through said queue stage.

4. A computer chipset as in claim 3, wherein said second circuit comprises:

a processing unit to process the tokens and data address information in said data queue and to generate control signals
5 for reordering the data in each packet;

a token buffer to receive one token from said token queue;
and

a reordering unit coupled to said processing unit and said token buffer and configured to reorder the data in each data
10 packet in the predetermined ordering, said reordering unit forming a pipeline with said processing unit to begin processing a token for one data packet while reordering of a preceding data packet is completing.

15 5. A computer chipset as in claim 1, wherein the predetermined ordering is a linear ordering that corresponds to sequential addresses of the data in the computer processor.

6. A computer chipset as in claim 1, wherein said second
20 circuit is coupled to output the ordered packets to a graphic controller through an accelerated graphic port.

7. A computer chipset as in claim 1, wherein the predetermined ordering is one of X86 orderings.

8. A computer system, comprising:

a computer processor;

a chipset coupled to said computer processor to control data
5 transfer and comprising an input data circuit and a reordering
circuit coupled to said input data circuit,

wherein said input data circuit processes address
information in received data associated with data addresses in
said computer processor to determine a received data ordering of
10 the received data based on the data addresses in said computer
processor, and said reordering circuit outputs data in a
predetermined ordering and maintains the address information of
the data regardless said received data ordering.

15 9. A computer system as in claim 8, wherein said chipset
receives input data in any one of four orderings in the Intel x86
ordering and outputs all data in a selected x86 ordering as said
predetermined ordering.

20 10. A computer system as in claim 8, wherein said input data
circuit comprises a token generator to receive and process the
address information of the data to generate tokens corresponding
to consecutive data packets, each token indicating at least the
received data ordering and addresses of data in a respective

packet.

11. A computer system as in claim 10, wherein said input
data circuit comprises a first signal path to transmit data and a
5 separate second signal path to transmit tokens.

12. A computer system as in claim 10, wherein said chipset
further comprises a queue stage having a token queue and a data
queue to respectively receive and store the tokens and the data
10 from said input data circuit, wherein said input data circuit and
said reordering circuit are connected to form a pipeline through
said queue stage.

13. A computer system as in claim 12, wherein said
15 reordering circuit comprises:

a processing unit to process the tokens and data address
information in said data queue and to generate control signals
for reordering the data in each packet;

a token buffer to receive one token from said token queue;
20 and

a reordering unit coupled to said processing unit and said
buffer and configured to reorder the data in each data packet in
the predetermined ordering, wherein said processing unit and said
reordering unit are connected to form a pipeline to begin

processing a token for one data packet while reordering of a preceding data packet is completing.

14. A computer system as in claim 8, further comprising an
5 accelerated graphic port chipset and said chipset is part of said accelerated graphic port chipset.

15. A computer system as in claim 8, further comprising:
a computer bus connected to said chipset; and
10 a computer device connected to said computer bus to receive data from said chipset.

16. A computer system as in claim 15, wherein said computer device is a graphic controller, the computer system further
15 comprising an accelerated graphic port between said chipset and said graphic controller to transfer data.

17. A computer system as in claim 8, further comprising a peripheral component interconnect (PCI) bus coupled to receive
20 output data from said chipset.